Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the aboveidentified application:

Listing of Claims

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Claims 1-37(Canceled).

Claim 38 (Currently Amended): A digital information coding apparatus, comprising:

- a) an input unit, arranged to selectively input first digital information data and second digital information data, the first digital information data being different from the second digital information data;
- b) a first encoder, arranged to encode the first digital information data and output parallel data of L bits;
- c) a second encoder, arranged to encode the second digital information data and output parallel data of M bits (L#M);
- d) a first converter, arranged to convert the parallel generate first data of L N bits generated by using a plural of the said first encoder, into first parallel data of N L bits $L \neq N$ generated by said first encoder;
- e) a second converter, arranged to convert the parallel generate second data of M N bits generated by using a plural of the said second encoder into second parallel data of N M bits (M≠N) generated by said second encoder;
- f) an error correction unit, arranged to selectively add an error correction check code to the first parallel data and the second parallel data,

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said error correction unit performing a common addition processing irrespectively of the first parallel data and the second parallel data.

Claim 39 (Previously Presented): An apparatus according to claim 38, wherein said first encoder encodes the first digital information data to be encoded by differential pulse code modulation.

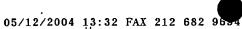
Claim 40 (Previously presented): An apparatus according to claim 38, wherein the second digital information data is a television signal in which a video signal and an audio signal are time-division multiplexed.

Claim 41 (Previously presented): An apparatus according to claim 38, further comprising a recording unit, arranged to record the data processed by said error correction unit on a recording medium.

Claim 42 (Previously presented): An apparatus according to claim 38, wherein the second digital information data being inputted in an amount less than the first digital information data during a predetermined period of time.

Claim 43 (Currently amended): A digital information coding method, comprising the steps of:

selectively inputting first digital information data and second digital information data, the first digital information data being different from the second digital information data; encoding the first digital information data to generate parallel data of L bits; encoding the second digital information data to generate parallel data of M bits (L#M); enverting the parallel generating first data of L N bits into first parallel by using a



plural of the data of N \perp bits (L \neq N);

converting the parallel generating second data of M bits into second parallel by using a plural of the data of N M bits (M≠N);

selectively adding an error correction check code to the first parallel data and the second parallel data, and

said error correction check code adding step performing a common addition processing irrespectively of the first parallel data and the second parallel data.